

REMARKS/ARGUMENTS

1. *Claims 1, 3-8 and 10-16 are rejected under 35 U.S.C. 102(b) as being anticipated by West et al. (US Patent 6,521,975 B1).*

5 **Response:**

Claim 1 recites a scribe line structure comprising a substrate, a plurality of dielectric layers formed on the surface of the substrate comprising at least a process monitor pattern set in a scribe line region, and a dummy metal structure formed on the surface of the substrate 10 connecting with the process monitor pattern and exposed in the **scribe line region.**

West provides a scribe street seals in semiconductor devices and method of fabrication. Please note that West particularly defines “dicing line” and “scribe street”: **The term “dicing line” is used to refer to the opening produced by the rotating saw separating the individual chips. The term “scribe street” is used to refer to the width of semiconductor material between the individual active circuits; consequently, this distance includes a length of semiconductor material surrounding each circuit and remaining with each chip after the separating dicing process. (col. 6, lines 8-15)** It is the most important premise according to West.

According to Fig. 1A of West, a substrate 140 is provided with a 25 plurality of dielectric layer 106 formed thereon. **A dicing line 110 between the edges of two chips generally designated 100 and 101.** The respective IC area terminated at the respective chip data edge; circuit 102 of chip 100

terminates at chip data edge 102a and is bordered by a length 104 of semiconductor material. Circuit 103 of chip 101 terminates at chip data edge 103a and is bordered by a length 105 of semiconductor material. It is noteworthy that **the sum of these lengths 104 and 105 plus the dicing line 110 is the distance between adjacent chip data edges 102a and 103a, and represents the “scribe street” 111 between the circuits 102 and 103.** Consequently only the materials in lengths 104 and 105 remain with their respective circuits. For this region of each respective chip, the term “seal region” will be used herein (col. 6, lines 46-64). **The scribe line region 111 indicated by the examiner in Page 2 of the detailed action actually comprises the dicing line 110 and the seal regions 104 and 105.**

West provides **at least two sets of substantially parallel seal structures within each of said seal regions 104 and 105.** Each of said sets comprises at least one continuous barrier wall adjacent each chip 100 and 101 respectively and at least one sacrificial composite structure in combination therewith, between said wall and the center of said dicing line 110. The composite structure is a discontinuous barrier wall comprising metal rivets interconnecting electrically conductive layers in an alternating manner, whereby the composite structure provides mechanical strength to said sets and simultaneously disperses the energy associated with crack propagation. (abstract)

It is noteworthy that the two sets of seal structures comprising continuous barrier wall and sacrificial composite structure are *located in the seal region 104 and 105, not in the dicing line 110.* Contrary to West, *the scribe line structure provided by the present application is located in the scribe line region.* It is well-known to those skilled in the art that the

scribe line region provided by the present application is where undergoes the chip singulation process and where each chip is individualized by a dicing apparatus. In other words, the scribe line region of the present application is similar with the dicing line 110 of West. Please note that **the seal structure of West is located in seal region 104 and 105 while the scribe line structure of the present application is located in the scribe line region (dicing line 110).**

Furthermore, West taught that the material in dicing line 110 is lost in the chip singulation process and consequently, only the materials in seal region 104 and 105 remain with their respective circuits. For this reason the seal structures **protecting the IC from propagating cracks and impurities (col. 6, lines 60-65)** by **offering mechanical strengths** are located in the seal region 104 and 105 around the peripheral of each chip. West particularly described that their seal structure is **NOT** in the dicing region 110. Difference from West, the scribe line structure of the present application is located in the scribe line region **for releasing heat and energy from the scribe line region to prevent chip cracks due to lateral explosion.** Therefore the applicant asserts that the seal structure of West and the scribe line structure of the present application are different structures located in different positions.

In summary, there are three differences between West and the present application:

- 25 (a) The scribe line region 111 indicated by the examiner in Page 2 of the detailed action comprises the dicing line 110 and the seal regions 104 and 105 while the scribe line region provided by the present application is

equal to the dicing line 110 merely.

(b) The seal structures of West are located in seal region 104 and 105 while the scribe line structure of the present application is located in the scribe line region (dicing line 110).

(c) The seal structure of West protects the IC from propagating cracks and impurities by offering mechanical strengths while the scribe line structure of the present application protects the IC chip from chip cracks by 10 releasing heat and energy from the scribe line region.

The applicant asserts that West does not teach the scribe line structure as per the limitation disclosed in claim 1 of the present invention. Therefore reconsideration of claim 1 is respectfully requested.

15 Claims 3-5 and 7 are dependent on claim 1 and should be allowed if claim 1 is allowed. Therefore reconsideration of claims 3-5 and 7 is politely requested.

20 With respect to claim 6, which recites that the process monitor pattern comprises test keys, feature dimension measuring elements, or alignment marks. The applicant appreciated that the cited paragraph is particularly pointed out by the examiner. However, col. 9, lines 63-65 of West describes that the width of the trenches for the continuous metal structure and the 25 width of the columns for the discontinuous seal structure is typically in the range from 0.2 to 0.4 μ m in the earlier layers. These widths may gradually widen in successive layer for easier alignment. The applicant also found that West never taught or suggested the seal structure could

comprise test keys, feature dimension measuring elements, or alignment marks. Therefore the present application is distinctly different from West, and reconsideration of claim 6 is politely requested.

5 With respect to claim 8, which recites a scribe line structure comprising a substrate with its surface comprising at least a scribe line region, a plurality of dielectric layers formed on the surface of the substrate comprising at least a process monitor pattern set in the scribe line region, and a heat irradiative structure formed in the plurality of dielectric 10 layers connecting the plurality of dielectric layers with the surface of the substrate and exposed **in the scribe line region**.

As mentioned above, West provides a scribe street seals in semiconductor devices and method of fabrication. West particularly 15 defined “dicing line” and “scribe street”: The term “dicing line” is used to refer to the opening produced by the rotating saw separating the individual chips. The term “scribe street” is used to refer to the width of semiconductor material between the individual active circuits. (col. 6, lines 8-15). And as shown in Fig. 1A, **the sum of these lengths 104 and 105 plus the dicing line 110 is the distance between adjacent chip data edges 102a and 103a, and represents the “scribe street” 111 between the circuits 102 and 103.** The scribe line region 111 indicated by the examiner in Page 2 of the detailed action actually comprises the dicing line 110 and the seal regions 104 and 105 while **the scribe line region provided by the 20 present application is equal to the dicing line 110 merely.**

It is noteworthy that the two sets of **seal structures comprising continuous barrier wall and sacrificial composite structure are located**

in the seal region 104 and 105, not in the dicing line 110. Contrary to West, the heat irradiative structure provided by the present application is located in the scribe line region. In addition, since the material in the dicing line 110 is lost in the chip singulation process and consequently 5 only the materials in seal region 104 and 105 remain with their respective circuits, (col. 6, lines 60-65) the seal structures of West protecting the IC from propagating cracks and impurities by offering mechanical strengths (abstract) is located in seal regions 104 and 105. West particularly described that their seal structure is NOT in the dicing region 10 110. Difference from West, the heat irradiative structure of the present application is located in the scribe line region for releasing heat and energy from the scribe line region to prevent chip cracks due to lateral explosion.

15 Based on those differences, the applicant asserts that the seal structure of West and the heat irradiative structure of the present application are different structures located in different positions, and West does not teach the scribe line structure as per the limitation disclosed in claim 8 of the present invention. Therefore reconsideration of claim 8 is respectfully 20 requested.

Claims 10-14 and 16 are dependent on claim 8 and should be allowed if claim 8 is allowed. Therefore reconsideration of claims 10-14 and 16 is politely requested.

25 With respect to claim 15, which recites that the process monitor pattern comprises test keys, feature dimension measuring elements, or alignment marks. The applicant appreciated that the cited paragraph is particularly

Appl. No. 10/710,761
Amdt. dated May 24, 2007
Reply to Office action of April 03, 2007

pointed out by the examiner, however, as mentioned above, col. 9, lines 63-65 of West describes width limitation of the trenches for the continuous metal structure and the width of the columns for the discontinuous seal structure. The applicant also found that West never taught or suggested the 5 seal structure could comprise test keys, feature dimension measuring elements, or alignment marks. Therefore the present application is distinctly different from West, and reconsideration of claim 15 is politely requested.

10 2. *Claims 2 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over West in view of Chooi et al. (US Patent 6,284,657 B1)*

Response:

15 Claims 2 and 9 are dependent on claims 1 and 8, respectively, and should be allowed if claims 1 and 8 are allowed. Therefore reconsideration of claims 2 and 9 is politely requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

20

25

Appl. No. 10/710,761
Amdt. dated May 24, 2007
Reply to Office action of April 03, 2007

Sincerely yours,

Winston Hsu

Date: 05.24.2007

Winston Hsu, Patent Agent No. 41,526

5 P.O. BOX 506, Merrifield, VA 22116, U.S.A.

Voice Mail: 302-729-1562

Facsimile: 806-498-6673

e-mail : winstonhsu@naipo.com

10 Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)